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| 09/992,064 | 11/21/2001 | Ashley Saulsbury | 188440/US | 4869 |

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* ASHLEY SAULSBURY and DANIEL S. RICE

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Appeal 2008-3103
Application 09/992,064[1]
Technology Center 2100

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Decided:[2] February 27, 2009

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*Before* JEAN R. HOMERE, JAY P. LUCAS, and THU A. DANG, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed November 21, 2001. The real party in interest is Sun Microsystems, Inc.

[2] The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

## STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1 through 21 under authority of 35 U.S.C. § 134. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to an improved method and apparatus for performing pixel averaging, as may be used in video processing. In the words of the Appellants:

> The present invention provides a novel computer processor chip having a sub-instruction for performing pixel average functions in parallel. As one skilled in the art will appreciate, performing multiple pixel average functions in a single instruction issue increases efficiency. Additionally, rounding the average up or down is possible in each sub-instruction to accommodate different rounding methodologies.

(Spec. 3, ll. 1-5).

Claim 1 is exemplary:

1. A method for averaging two pixel values, comprising:

decoding a single machine code instruction comprising an address for a first input register, an address for a second input register, an address for an output register, an op code indicating a function to perform, and a rounding factor;

loading a plurality of first operands from the first input register;

loading a plurality of second operands from the second input register;

producing an average, based on the op code, of one of the plurality of first operands and one of the plurality of second operands, wherein the rounding factor indicates which of a plurality of rounding algorithms to use in producing the average, the plurality of rounding algorithms comprising:

> a first rounding algorithm able to produce a change in the average; and

a second rounding algorithm able to produce a change in the average; and

storing the average in the output register.

## PRIOR ART

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

| | | |
|---|---|---|
| Sijstermans | 6,889,242 B1 | May 3, 2005 |

## REJECTION

Claims 1 through 21 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Sijstermans.

Appellants contend that the claimed subject matter is not anticipated by Sijstermans because Sijstermans fails to teach an important claimed limitation, as will be explained below. The Examiner contends that each of the claims is properly rejected.

We reverse the rejection.

## ISSUE

The principal issue before us is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e). The issue turns on whether Sijstermans teaches a single instruction comprising a rounding factor, as claimed.

## FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a method and apparatus for averaging the values of pixel very quickly, as needed for video processing. (Spec. 1, bottom paragraph). The method uses Very Long Instruction Word (VLIW) processors, of 128 bits (for example), which process the VLIW instructions. (*Id.* at 1, l. 25). These instructions are divided into four sub-instructions of 32 bits each, each sub-instruction controlling one parallel processor and supplying it with an operation code, two operand fields with the addresses of the operands to be averaged, a field with the address of the register into which to deposit the result, and a rounding factor. (Fig. 4, Spec. 8).

2. The reference patent Sijstermans teaches various methods for performing rounding operations while machine instructions are being processed in a computer. (Col. 1, ll. 45-54). The exact mode of rounding can be one of at least 8 types of rounding, as demonstrated in the Table 1 (col. 5, l. 30). The method includes one instruction to set the rounding mode, and a second instruction to generate a result rounded according to the rounding mode. (Col. 1, l. 67).

## PRINCIPLES OF LAW

"In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) "In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art." *Id.* (internal citations omitted).

> [U]nless a reference discloses within the four corners of the document not only all of the limitations claimed *but also all of the limitations arranged or combined in the same way as recited in the claim*, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.

*Net MoneyIN, Inc. v. VeriSign et al.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) (emphasis added).

## ANALYSIS

From our review of the administrative record, we find that Examiner has presented a prima facie case for the rejection of Appellants' claims under 35 U.S.C. § 102(e). The prima facie case is presented on pages 4 to 9 of the Examiner's Answer. In opposition, Appellants present the following argument.

*Arguments with respect to the rejection of claims 1 to 21 under 35 U.S.C. § 102(e)*

Claim 1, and indeed all of the claims, recite in relevant part "decoding a single machine code instruction comprising an address for a first input register . . . and a rounding factor." Appellants contend that the Examiner erred in rejecting claims 1 to 21 as being anticipated by Sijstermans because "Sijstermans simply fails to disclose that the rounding factor is included in the same instruction [as the register addresses and op codes]." (App. Br. 7, bottom).

Examiner submits that the single VLIW instruction including a rounding factor is taught in a number of places in the Sijstermans patent. (Answer 11, second paragraph). We have reviewed all of these particular cites referred to by the Examiner, as well as the entire reference, and we do not find the teaching in Sijstermans needed to anticipate the claims. To the contrary, we find that apart from the first instruction executed to set a rounding mode, Sijstermans discloses executing a second instruction to round a generated integer result. Particularly, Sijstermans states:

> "In one embodiment, the invention is directed to a method in which a first instruction is executed in a programmable processor to set a rounding mode. A second instruction is executed within the programmable processor to generate an integer result rounded according to the rounding mode."

(Sijstermans, col. 1, ll. 63-67). Thus, we agree with Appellants that Sijstermans execute two separate instructions to decode the rounding code whereas the claim requires the execution of a single instruction to decode the

rounding code. Without the requisite support in the reference of record, we cannot affirm a rejection of anticipation under 35 U.S.C. § 102(e).

## CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have shown that the Examiner erred in rejecting claims 1 to 21.

## DECISION

We reverse the Examiner's rejection of claims 1 to 21.

## REVERSED

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